AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A multi-layered real-time stereo matching apparatus comprising:

a left and a right image acquisition unit for obtaining a left and a right image of an object on a spatial area from different positions;

an image processing unit for converting the left and the right image to a left and a right digital image; and

a multi-layered image matching unit, which includes a systolic array, for comparing one scan line in one of the left and the right digital image with multiple scan lines in the other of the left and the right digital image in real-time by using the systolic array so that each pixel in the one scan line matches another pixel in the multiple scan lines in the other digital image,

wherein the multi-layered image matching unit receives pixels of the one scan line in the one digital image sequentially and receives pixels of the multiple scan lines in the other digital image at a time, and calculates a disparity between one pixel in the one scan line and said another pixel in the multiple scan lines,

wherein the systolic array includes a plurality of layers for receiving pixel data of the one scan line in the one digital image and receiving pixel data of the multiple scan lines in the other digital image one by one, wherein two adjacent layers exchange costs and active signals with each other and the multi layered image matching unit further includes an accumulator for accumulating data fed from the layers to generate the disparity,

wherein each of the layers has:

a first storing unit for storing pixels of the left digital image;

a second storing unit for storing pixels of the right digital image; and

a plurality of forward processors, stacks and backward processors for generating decision values and the disparity obtained from the left and the right digital image based on a clock signal,

wherein each of the backward processors of said each of the layers includes:

an OR gate for logically summing two active bit paths inputted from an upper and a lower backward processor in said each of the layers, two active bit paths inputted from an upper and a lower layer of said each of the layers and a recursive active bit path within said each of the backward processors to generate a logical sum of five active bit paths;

an activation register for storing the logical sum of five active bit paths;

a demultiplexor for demultiplexing the logical sum of five active bit paths based on a decision value fed from the stack; and

a tri-state buffer for outputting the decision value in case the logical sum of five active bit paths in the activation register is high, and

wherein said left and right digital images are left and right images of said object, and wherein matching the pixel in the one scan line with another pixel in the multiple scan lines enables location of the object in said spatial area so that the imprecision in location and direction of, or distortion caused by, said left and right image acquisition unit is prevented.

2-9. (Canceled)

10. (Currently Amended) The apparatus of claim ~~6~~ 1, wherein an activation register of all layers of which 0-th backward processor has a minimum cost is initialized to be activated and all activation registers of other backward processors are initialized to be inactivated.

11. (Currently Amended) The apparatus of claim ~~6~~ 1, wherein the backward processor accumulates the decision values fed from the tri-state buffer on a step basis to provide an optimized disparity and an optimized layer number.

12. (Previously Presented) The apparatus of claim 11, wherein the backward processor uses the layer number to search a scan line from multiple scan lines of the other digital image that corresponds to one scan line of the one digital image and uses the optimized disparity to search a pair of pixels, the two pixels corresponding to each other in the right and the left digital image on a backward processing step basis.

13. (Previously Presented) The apparatus of claim 11, wherein the backward processor initializes the disparity to be 0 on a layer basis and adds on a step basis to the disparity the decision values fed from a backward processor which is located in the layer corresponding to the layer number fed on a step basis during a backward processing and has a processing element number same as the disparity value.

14-15. (Canceled)

16. (Currently Amended) The apparatus of claim ~~6~~ 1, wherein the imprecision in location and direction of, or the distortion caused by, said left and right image acquisition unit is prevented even though said left and right image acquisition unit are arranged such that the one scan line and the multiple scan lines are not parallel.